

SMART POWER 3-PHASE MOTOR DRIVE FOR SPACE APPLICATIONS

DESCRIPTION

The PWR-82332 is a Smart Power 3-phase Motor Drive hybrid. The PWR-82332 uses a MOSFET output stage with 400 VDC rating, and can deliver 19A continuous current to the load. Individual fast recovery diodes are internally connected across each of the six output transistors to clamp inductive flyback. High and low-side input logic signals are XOR'd in each phase to prevent simultaneous turn on of in-line transistors, thus eliminating a shoot thru condition. The internal logic controls the high and low-side gate drives for each phase and operates from 5 V logic levels. The internal power supply provides a constant voltage source to the floating high-side gate drives. This provides constant output performance for switching frequencies from dc to 50 kHz.

APPLICATIONS

Packaged in a small case, this hybrid is an excellent choice for high performance, high-reliability motor drives for servo-amps and speed controls. Among the many applications are robotic arms; electro-mechanical valve assemblies; actuator systems; antenna and solar panel positioning; fan and blower motors for environmental conditioning; Reaction wheels; compressor motors for cryogenic coolers. The PWR-82332 hybrid is ideal for harsh military/space environments where shock, vibration, and temperature extremes are evident. The PWR-82332 operates over the -55°C to +125°C temperature range and is available with K-Level processing.

FEATURES

- **Small Size (3.0" x 2.3" x 0.40")**
- **400 VDC Rating**
- **19 A Continuous Current Capability**
- **Class K Processing**
- **SEU Immune for LET Level of 36 MeV/mg/cm²**
- **Can Withstand 10 KRad (Si) Total Dose Radiation**
- **Space Station Qualified Drawing #SSQ22691**
- **High-Efficiency MOSFET Drive Stage**
- **Direct Drive for Commutation Logic**
- **6 Step Trapezoidal or Sinusoidal Drive**
- **Four Quadrant Operation**

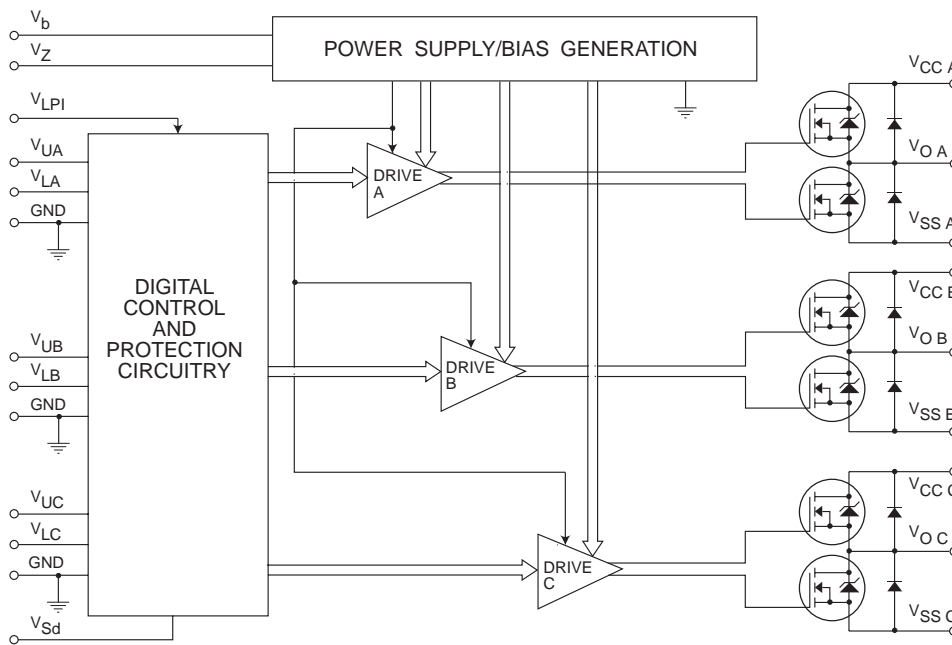


FIGURE 1. PWR-82332 BLOCK DIAGRAM

**TABLE 1. ABSOLUTE MAXIMUM RATINGS (SEE NOTE 1)
(TC = +25°C UNLESS OTHERWISE SPECIFIED)**

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage (see note 2)	V _{cc}	400	VDC
Bias Voltage	V _b	50	VDC
Logic Power-In Voltage	V _{LPI}	5.5	VDC
Input Logic Voltage	V _U , V _L , V _{sd}	6.0	VDC
Output Current			
Continuous	I _o	19	A
Pulsed (f _o = 50kHz, duty cycle = 5%, V _{cc} = 120V)	I _{oP}	25	A
Operating Frequency	f _o	50	kHz
Case Operating Temperature	T _c	-55 to +125	°C
Storage Temperature Range	T _{cs}	-65 to +150	°C
GND-V _{ss} Differential Voltage		±3V	VDC or peak
Dielectric Withstanding Voltage (all pins to package)	DMV	500	VDC

**TABLE 2. PWR-82332 SPECIFICATIONS
(TC = +25°C UNLESS OTHERWISE SPECIFIED)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT						
Output Current Continuous	I _o				19	A
Supply Voltage	V _{cc}			120	400	V
Output On-Resistance (each FET; see FIGURE 13)	R _{on}	I _F = 15A (see note 1)			0.25	Ohm
Instant Forward Voltage (Flyback diode; see FIGURE 12)	V _F	I _F = 15A (see note 1)			1.6	V
Reverse Recovery Time (Flyback diode)	t _{rr}	I _F = 1A, I _R = 1A			50	nsec
Reverse Leakage Current at T _c = +25°C	I _R	V _{cc} = 400V, V _U = V _L = Logic 0			280	µA
Reverse Leakage Current at T _c = +125°C	I _R	V _{cc} = 400V, V _U = V _L = Logic 0			7	mA
BIAS SUPPLY						
Input Bias Supply (T _c = -55°C to +125°C)	V _b		14		50	V
Quiescent Bias Current (see note 2)	I _{bq}	V _b = 28V		40		mA
Bias Current (T _c = -55°C to +125°C; see FIGURES 9, 10, 11)	I _b	V _b = 28V, f _o = 30kHz			100	mA
Inrush Current (T _c = -55°C to +125°C)	I _{ir}	V _b = 28V			1.4	A
Logic Power Input Current	I _{LPI}	V _{LPI} = 5.0V			7	mA
INPUT SIGNALS						
High-Level Input Voltage	V _{IH}		3.15			V
Low-Level Input Voltage	V _{IL}				0.9	V
SWITCHING CHARACTERISTICS (see FIGURE 2)						
Upper drive:						
Turn-on Propagation Delay	t _d (on)	I _o = 15A Peak			690	nsec
Turn-off Propagation Delay	t _d (off)	V _{cc} = 120V			1375	nsec
Shut-down Propagation Delay (see FIGURE 5)	t _{sd}				800	nsec
Turn-on Rise Time	t _r				300	nsec
Turn-off Fall Time	t _f				300	nsec
Lower drive:						
Turn-on Propagation Delay	t _d (on)				675	nsec
Turn-off Propagation Delay	t _d (off)				1050	nsec
Shut-down Propagation Delay (see FIGURE 5)	t _{sd}				700	nsec
Turn-on Rise Time	t _r				300	nsec
Turn-off Fall Time	t _f				300	nsec
MINIMUM PULSE WIDTH						
	tpw		175			nsec
THERMAL						
Maximum Thermal Resistance	θ _{j-c}				0.85	°C/W
Maximum Lead Soldering Temperature	T _s	see note 3			250	°C
Junction Temperature Range	T _j	each transistor	-55		150	°C
Case Operating Temperature	T _{co}		-55		125	°C
Case Storage Temperature	T _{cs}		-55		150	°C
WEIGHT						
					6.125 (175)	oz (g)

NOTES:

1. Pulse width ≤ 300µs, duty cycle ≤ 2%.
2. V_U, V_L = Logic '0' on pins 17, 18, 20, 21, 24 and 25.
3. Solder 1/8" from case for 5 seconds maximum.

INTRODUCTION

The 3-Phase PWR-82332 is a 19A motor drive rated at 400V. The PWR-82332 uses a MOSFET output stage for high speed, high current, and high-efficiency operation. This motor drive is ideal for use in high-performance motion control systems, servo amplifiers, and motor speed control designs. Furthermore, multi-axis systems requiring multiple drive stages can benefit from the small size of this power drive.

The PWR-82332 can be driven directly from commutation logic, DSP, or a custom ASIC that supplies digital signals to control the upper and lower transistors of each phase. This highly integrated drive stage has digital inputs that control the high and low side of each phase. Digital protection of each phase eliminates an in-line firing condition, by preventing simultaneous turn-on of both the upper and lower transistors in a given phase. The PWR-82332 has a ground referenced low-side gate drive. An internal dc-dc converter supplies a floating output to each of the 3 high side drives.

This provides a continuous high-side gate drive even during a motor stall. The high and low-side gate drivers control the N-channel MOSFET output stage. The MOSFETs used in the PWR-82332 allow output switching up to 50 kHz. A flyback diode parallels each output transistor and controls the regenerative energy produced by the motor. These fast recovery diodes have faster reverse switching times than the intrinsic body diode of the MOSFETs used in the PWR-82332. Care should be taken to adequately heatsink these motor drives to maintain a case temperature under 125°C. Junction temperatures should not exceed 150°C. The PWR-82332 does not have an internal short-circuit or overcurrent protection. For protection of the output transistors, these features must be added external to the hybrid.

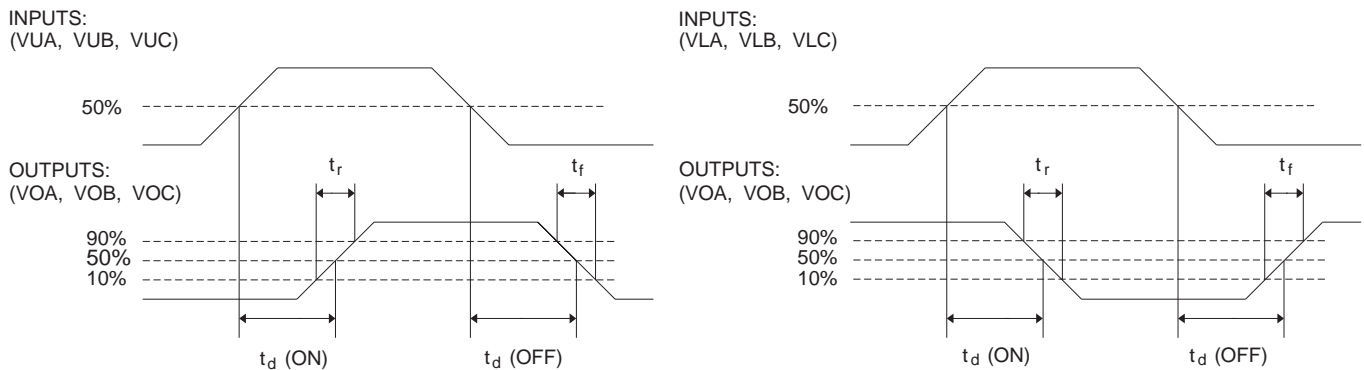


FIGURE 2. INPUT/OUTPUT TIMING RELATIONSHIPS

BIAS VOLTAGES

The PWR-82332 motor drive hybrid requires a single input bias supply for operation. The hybrid generates three independent, floating supplies internally, which eliminates the need for external bias voltages for each phase.

In order for the internal power supply to generate these voltages, the input bias voltages (V_b) must be from 15 to 50 Vdc.

Any voltage available in the system in the 15 to 50 Vdc range can be directly connected to the V_b pin of the hybrid. (See FIGURE 3).

A 0.01 μF decoupling capacitor must be connected between V_b (pin 12) and GND and VLPI (pin 16) to GND.

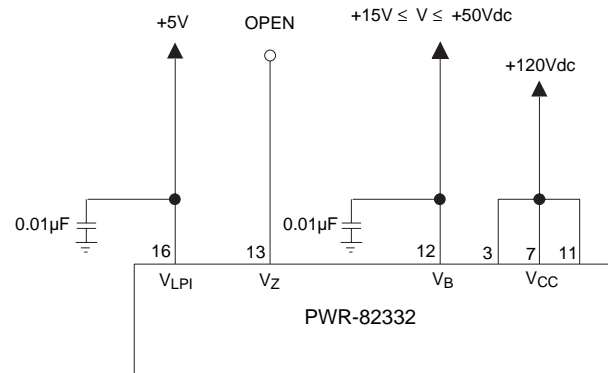


FIGURE 3. CONNECTION TO BUS VOLTAGE, INPUT BIAS VOLTAGE AND LOGIC POWER INPUT VOLTAGE

DIGITALLY CONTROLLED INPUTS

The PWR-82332 digital inputs can be driven with any type of 5 V logic, such as TTL or CMOS logic. PIN 16 is the logic power input (VLPI) for the digital circuitry inside the hybrid. An external 5 V power supply must be connected between this pin and GND. **A 0.01 μ F ceramic capacitor must be placed between this pin and GND as close to the hybrid as possible see (FIGURE 3).**

The commutation/control circuitry can be as simple as discrete logic with PWM, or as sophisticated as a microprocessor or custom ASIC, depending on the system requirements. The Block diagram in FIGURE 4 shows a typical interface of the PWR-82332 with a motor and commutation logic in a Servo-Amp System.

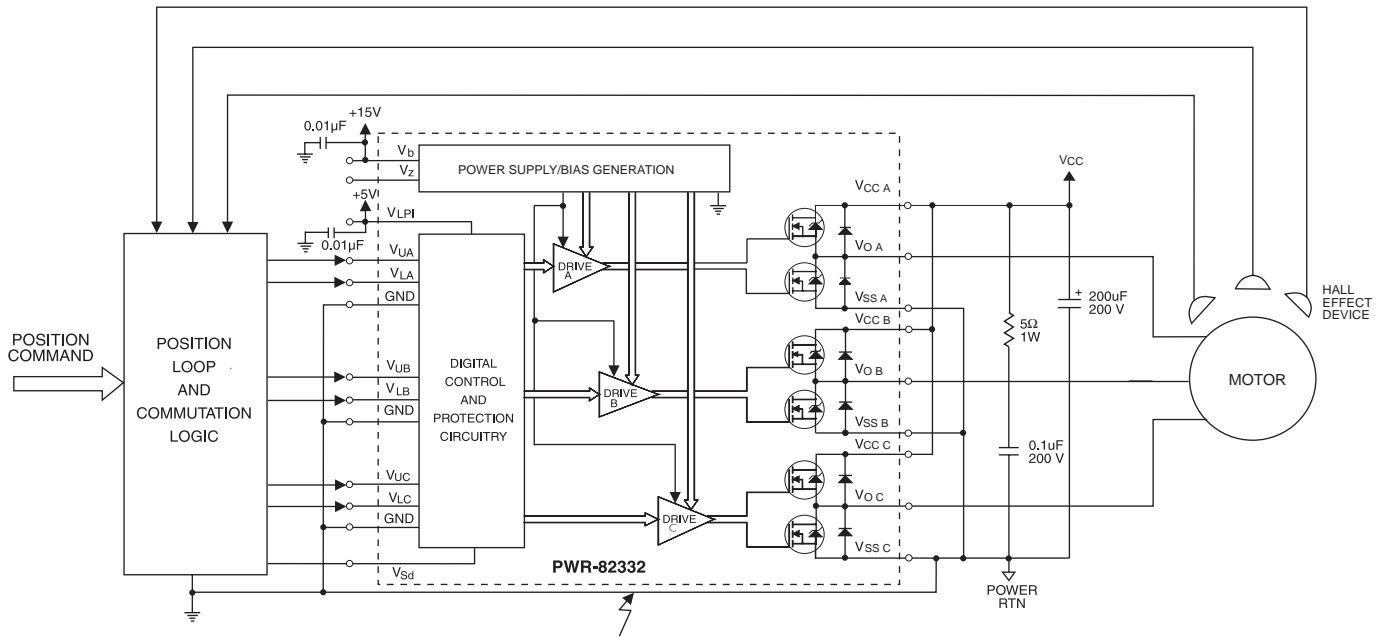
SHUT-DOWN INPUT (Vsd)

Pin 23 (Vsd) provides a digital shut-down input, which allows the user to completely turn off both the upper and lower output transistors in all 3 phases. Application of a logic '1' to the Vsd input will disable the Digital/Control Protection circuitry thereby turning off all output transistors. The circuitry remains disabled and will

not respond to signals on the VL or VU inputs while the Vsd has a logic '1' applied. See FIGURE 5. When the user or the sense circuitry (as in FIGURE 6) returns the Vsd input to a logic '0', the output transistors will respond to the corresponding digital input. This feature can be used with the external current limit or temperature sense circuitry to disable the drive if a fault condition occurs (see FIGURE 6).

INTERNAL PROTECTION CIRCUITRY

The hybrid contains digital protection circuitry, which prevents in-line transistors from conducting simultaneously. This, in effect, would short circuit the power supply and would damage the output stage of the hybrid. The circuitry allows only proper input signal patterns to cause output conduction. TABLE 3. shows these timing relationships. If an improper input requested that the upper and lower transistors of the same phase conduct together, the output would be a high impedance until removal of the illegal code from the input of the PWR-82332. A dead time is not required for the signals at the VU and VL pins.



CRITICAL GROUND PATH

To prevent damage to the internal drive circuitry, the differential voltage between GND (pins 19,22,26) and Vss (pins 1, 5, 8) must not exceed $\pm 3V$ max, dc or peak

FIGURE 4. PWR-82332 TYPICAL INTERFACE WITH A MOTOR

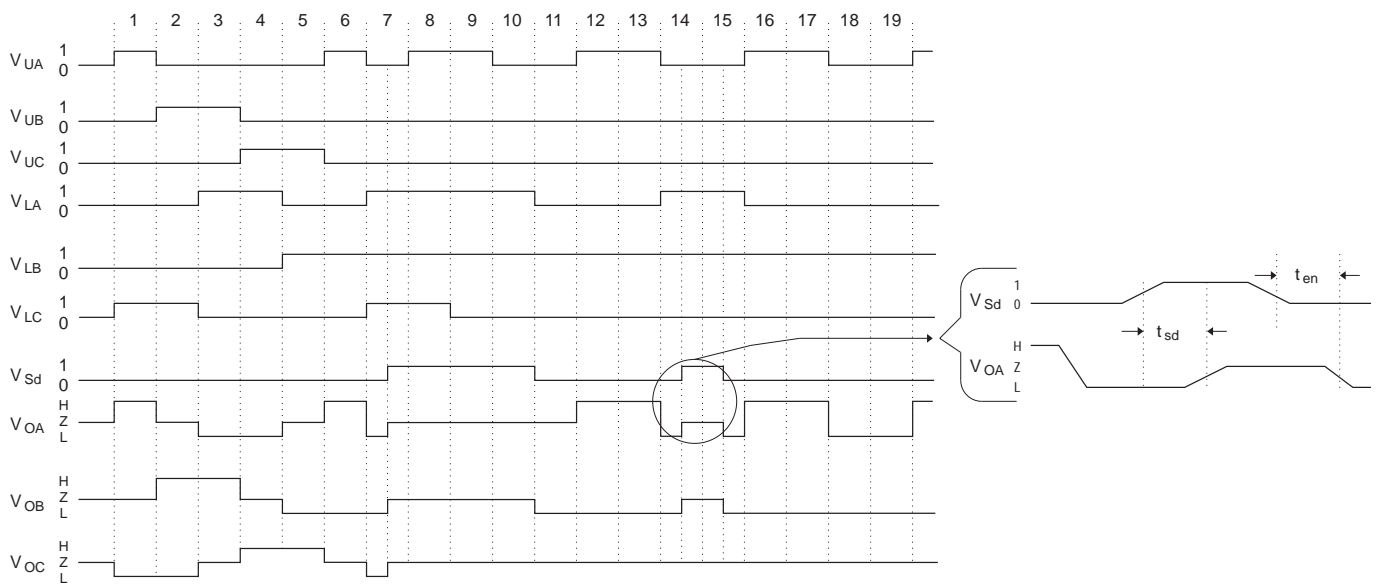


FIGURE 5. SHUT-DOWN (V_{sd}) TIMING RELATIONSHIP

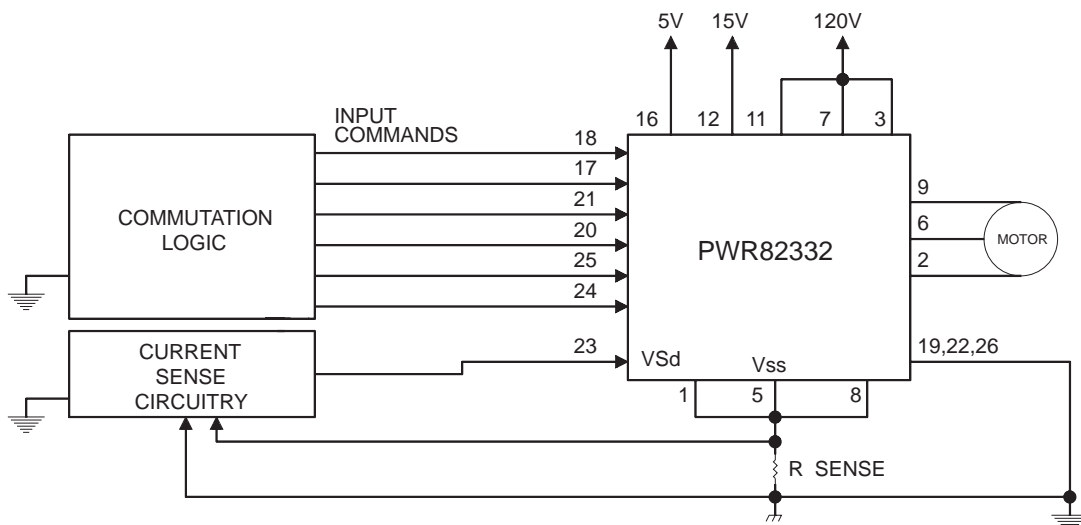


FIGURE 6. FUNCTIONAL SHUT-DOWN INPUT USED WITH CURRENT-SENSING CIRCUITRY

PWR-82332 POWER DISSIPATION (see FIGURE 7)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses. Consider the following operating conditions

V_{CC} = 120 V (Bus Voltage)
 I_{OA} = 10 A, I_{OB} = 12 A (see FIGURE 7)
 t_{on} = 30 μ s (see FIGURE 7); T = 40 μ s (period)
 R_{on} = 0.51 Ω (on-resistance, Assume worst case, T_j = +150°C)
 (see Figure 13)

t_{s1} = 600 ns; t_{s2} = 300 ns (see FIGURE 7)
 f_o = 25 kHz (switching frequency)
 V_F is the diode forward voltage, I_o = 12 A, T_C = +25°C
 V_F (avg) = 0.95 V; I_F is the diode forward current

1. Conduction Losses (P_C)

$$P_C = (I_{motor\ rms})^2 \times R_{on}$$

$$I_{motor\ rms} = \sqrt{\left(I_{OB}^2 - I_{OB}(I_{OB} - I_{OA}) + \frac{(I_{OB} - I_{OA})^2}{3} \right) \left(\frac{t_{on}}{T} \right)}$$

$$I_{motor\ rms} = \sqrt{\left(12^2 - 12(12 - 10) + \frac{(12 - 10)^2}{3} \right) \left(\frac{30}{40} \right)}$$

$$P_C = (9.54)^2 \times (0.51\Omega) = 46.42\text{ Watts}$$

2. Switching Losses (P_S)

$$P_S = [V_{CC} (I_{OA}) (t_{s1}) + I_{OB} (t_{s2})] f_o / 2$$

$$P_S = [120 (10 (600\text{ ns}) + 12 (300\text{ns})) 25\text{kHz}] / 2$$

$$P_S = 14.4\text{ Watts}$$

3. Flyback diode Losses (P_d)

$$P_d = I_f (avg) \times V_f (avg)$$

$$I_f (avg) = [(I_{OB} + I_{OA}) / 2] / 2$$

$$= [(12 + 10) / 2] / 2 = 5.5\text{ A}$$

$$P_d = 5.5\text{ A} \times 0.95\text{ V}$$

$$P_d = 5.23\text{ Watts}$$

Transistor Power Dissipation (P_T)

To calculate the maximum power dissipation of the output transistor / diode pair as a function of the case temperature, use the following equation. (Reference FIGURE 14 to ensure you don't exceed the maximum allowable power dissipation of each transistor / diode pair.)

$$P_T = P_C + P_S + P_d$$

In this example, $P_T = 46.42 + 14.4 + 5.23 = 66.05\text{ Watts}$

Total Hybrid Power Dissipation (P_{Hybrid})

To calculate Total Power Dissipated in the hybrid add the power dissipation of each conducting transistor / diode pair. Typically, only two transistor / diode pairs are conducting at any given time.

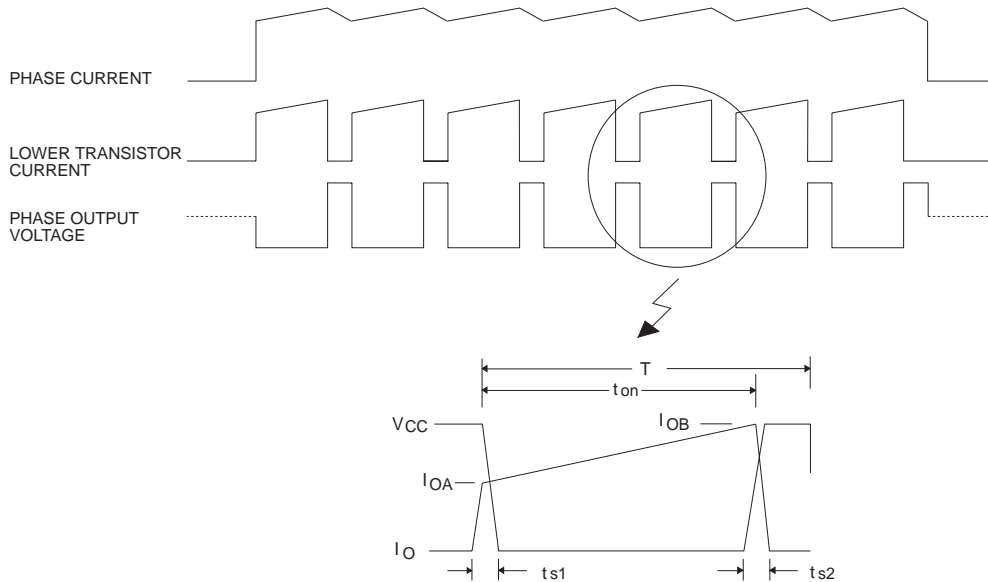


FIGURE 7. OUTPUT CHARACTERISTICS

GROUND CONNECTIONS

LAYOUT AND EXTERNAL COMPONENTS

Important Information - The following layout guidelines and required external components are critical to the proper operation of this motor drive.

Permanent damage will result to the motor drive if the user does not make the following recommended ground connections that will ensure the proper operation of the hybrid.

The V_b , V_{LPI} and logic ground returns are on pins 19, 22, and 26 (GND). The V_{SS} connections for the output stage are on pins 1, 5, and 8 (Vss). **To prevent damage to the internal drive circuitry, the differential voltage between GND (pins 19, 22, 26) and V_{SS} (pins 1, 5, 8) must not exceed ± 3 V max, dc or peak.** This includes the combined voltage drop of the associated ground paths and the voltage drop across R_{SENSE} (see FIGURES 6 and 8).

For example, a value of R_{SENSE} of 0.025Ω will give a voltage drop of 0.375 V at 15 A, and allow enough margin for the voltage drop in the ground conductors. Locate R_{SENSE} 1 IN. to 2 IN. maximum from the hybrid. **It is critical that all ground connections be as short, and of lowest impedance, as the system allows.**

$C1$ and $C2$ are $0.01\mu\text{F}$ power supply decoupling capacitors.

Care must be taken to control the regenerative energy produced by the motor in order to prevent excessive voltage spiking on the V_{CC} line. Accomplish this by placing a Tantalum capacitor or clamping diode between V_{CC} and the high power ground return.

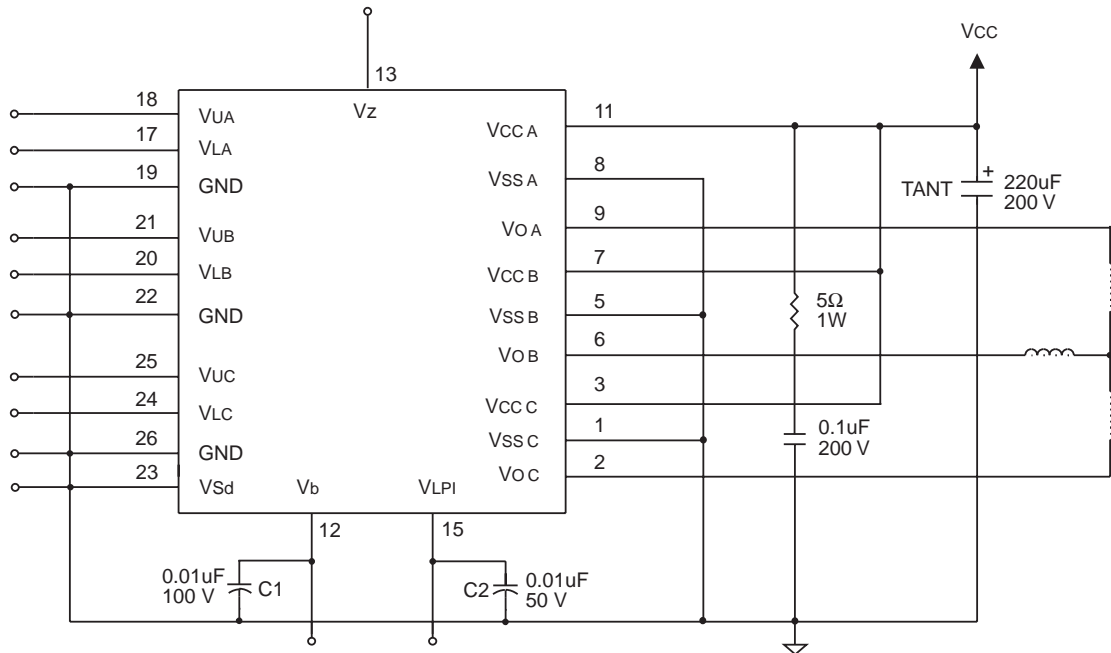
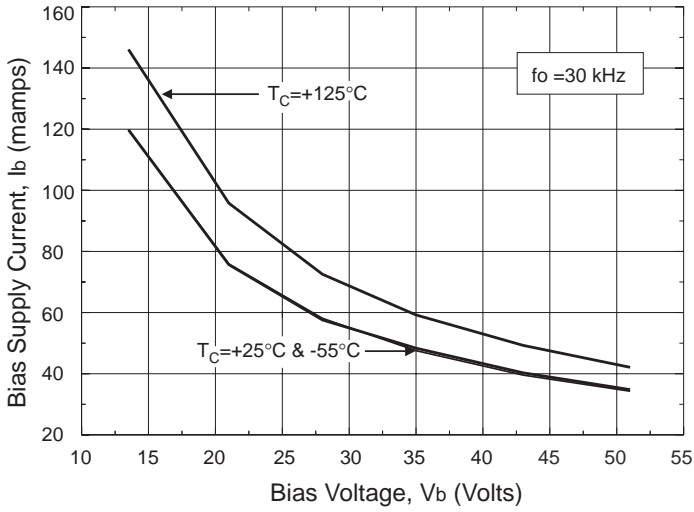
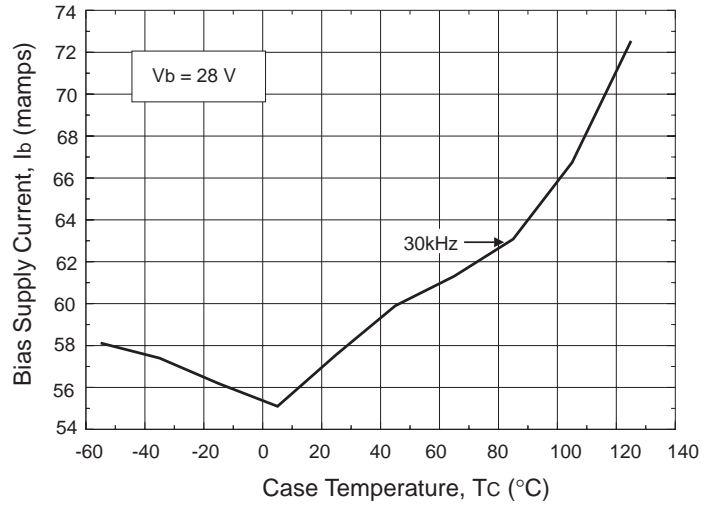


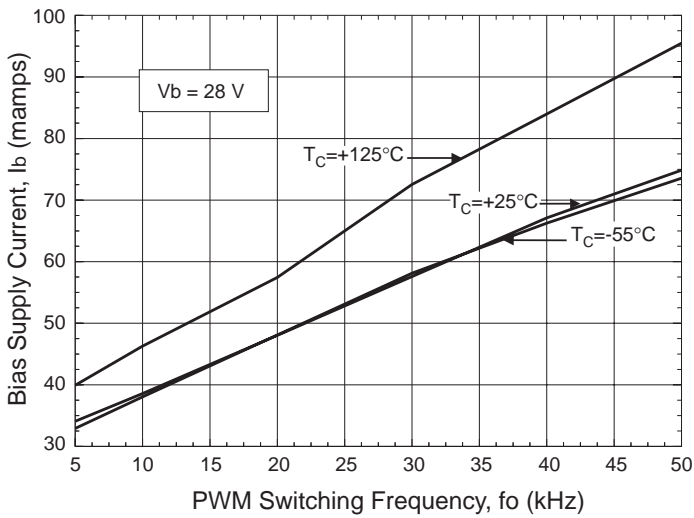
FIGURE 8. PWR-82332 GROUND CONNECTION



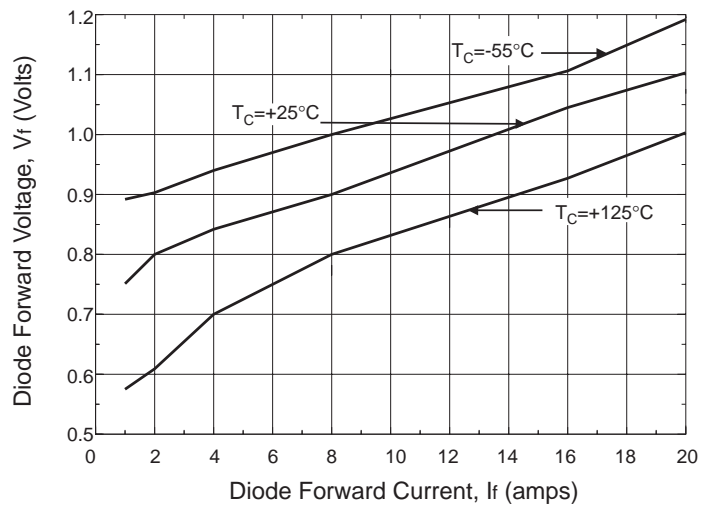
**FIGURE 9. PWR-82332
BIAS SUPPLY CURRENT VS. BIAS VOLTAGE**



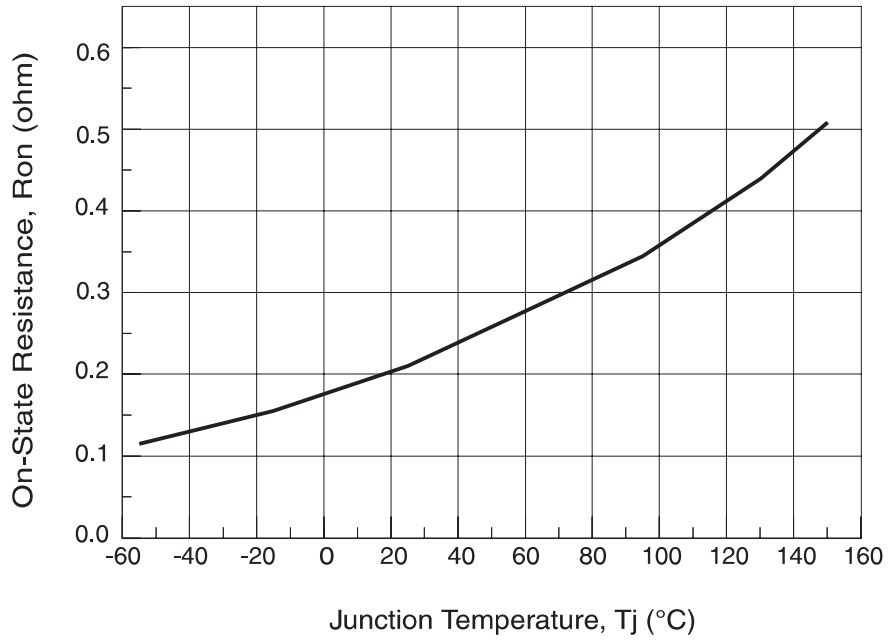
**FIGURE 10. PWR-82332
BIAS SUPPLY CURRENT VS. CASE TEMPERATURE
@ fo = 30kHz**



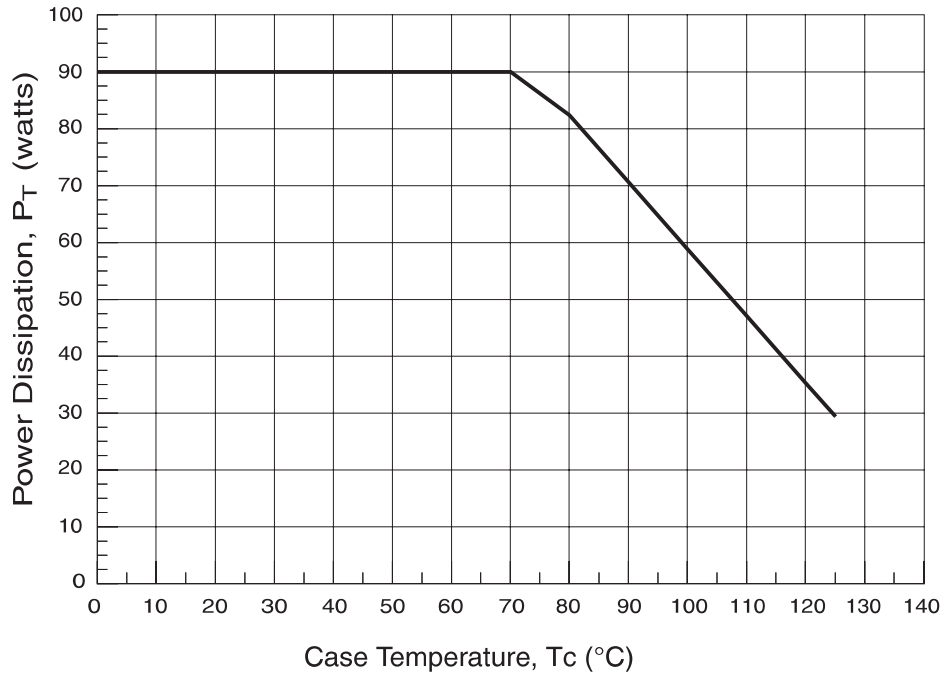
**FIGURE 11. PWR-82332
BIAS SUPPLY CURRENT VS. PWM SWITCHING
FREQUENCY**



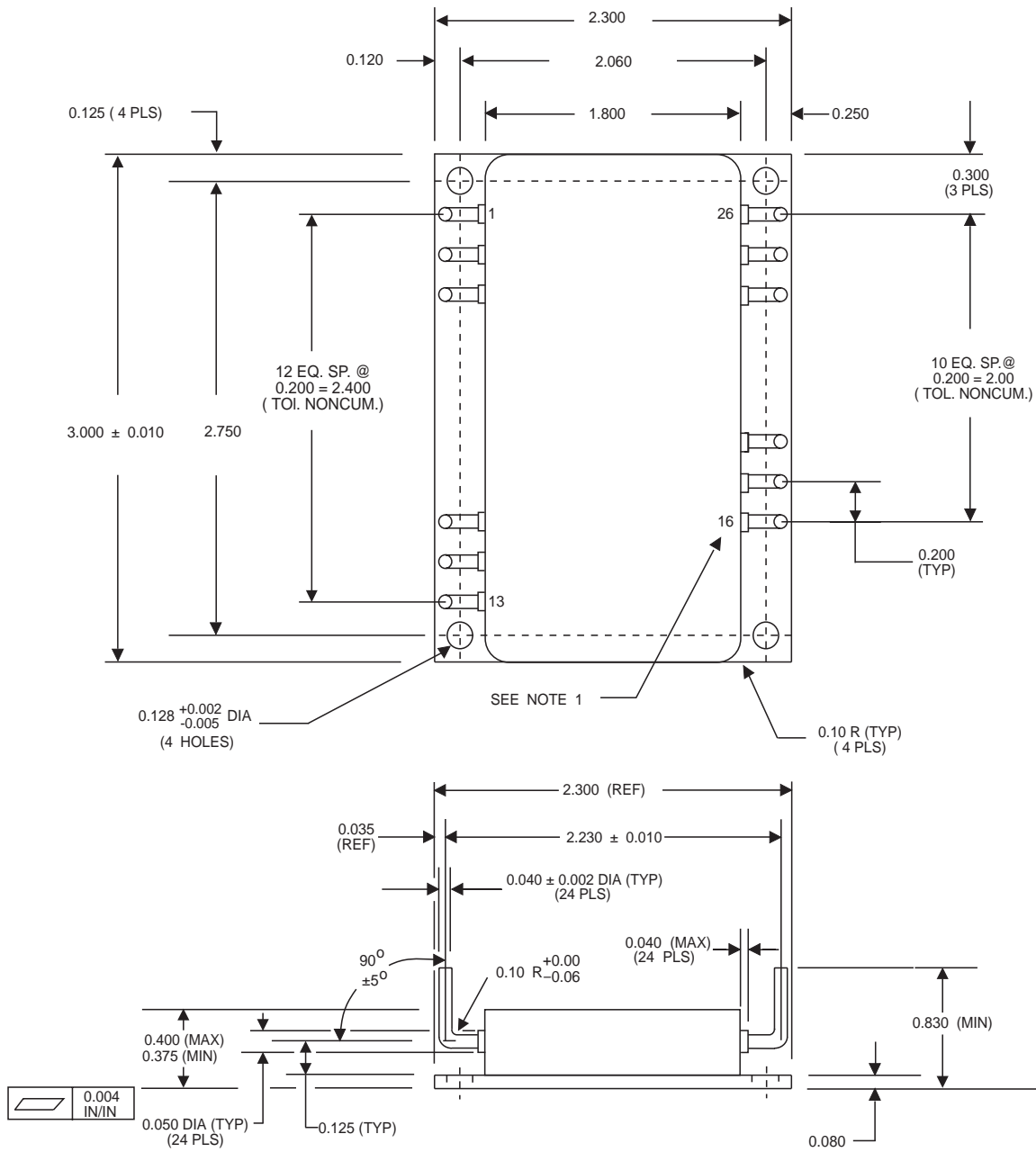
**FIGURE 12. PWR-82332
DIODE FORWARD VOLTAGE VS. DIODE FORWARD
CURRENT**



**FIGURE 13. PWR-82332
ON-STATE RESISTANCE VS. JUNCTION TEMPERATURE**

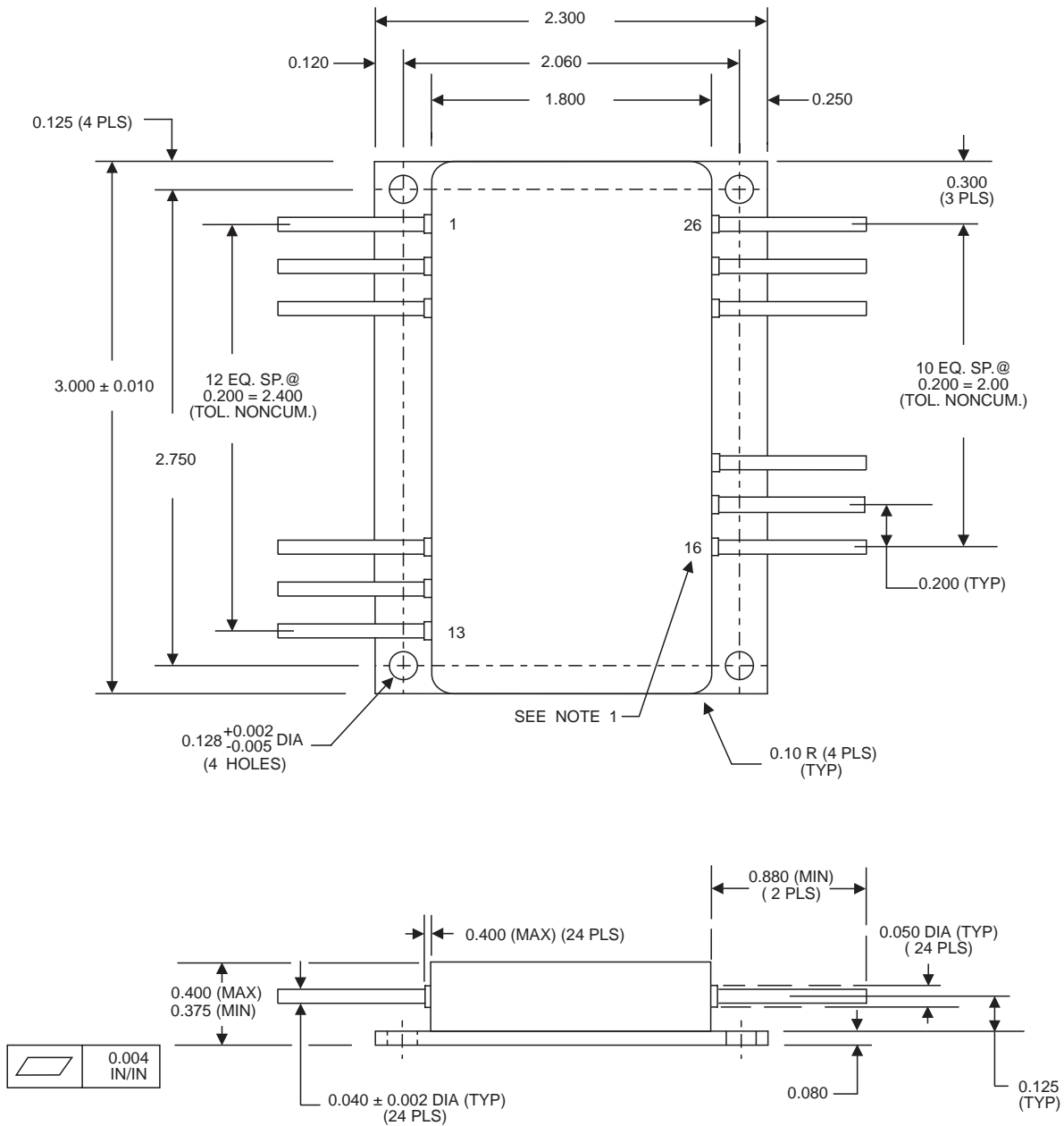


**FIGURE 14. PWR-82332
POWER DISSIPATION VS. CASE TEMPERATURE**



- NOTES:
1. Pin 1 is marked on lid. All other pin numbers are for reference only and do not appear on package.
 2. Tolerance, unless otherwise specified: X.XXX = ± 0.005, X.XX = ± 0.01.
 3. All dimensions are in inches unless otherwise specified.
 4. Material:
 Frame: Stainless Steel 304
 Base: Glid Copper
 Lead: OFHC Copper
 Cover: Stainless Steel 304

FIGURE 15B. CASE OUTLINE Y



NOTES:

1. Pin 1 is marked on lid. All other pin numbers are for reference only and do not appear on package.
2. Tolerance, unless otherwise specified: X.XXX = ±0.005, X.XX = ±0.01
3. All dimensions are in inches, unless otherwise specified.
4. Material:
 - Frame: Stainless Steel 304
 - Base: Glid Copper
 - Lead: OFHC Copper
 - Cover: Stainless Steel 304

FIGURE 15C.CASE OUTLINE Z

MOUNTING

The package bolts to part of the chassis or even the motor assembly itself, depending on system requirements. In applications where this isn't convenient, the hybrid can be mounted to its own heatsink. The heat transfer in a hybrid is from semiconductor junction to the bottom of the hybrid case. The flatness and maximum temperature of this mounting surface are critical to proper performance and reliability, because this is the only method of dissipating the power created in the hybrid. Use a mounting surface flatness of 0.004 inches/inch maximum. This interface can be improved with the use of a thermal compound or pad. The heatsink should be designed to insure that the temperature does not exceed +125°C.

TABLE 3. INPUT-OUTPUT TRUTH TABLE									
INPUTS							OUTPUTS		
UPPERS			LOWERS			CONTROL			
V _{UA}	V _{UB}	V _{UC}	V _{LA}	V _{LB}	V _{LC}	V _{sd}	V _{OA}	V _{OB}	V _{OC}
1	0	0	0	1	0	0	H	L	Z
1	0	0	0	0	1	0	H	Z	L
0	1	0	0	0	1	0	Z	H	L
0	1	0	1	0	0	0	L	H	Z
0	0	1	1	0	0	0	L	Z	H
0	0	1	0	1	0	0	Z	L	H
0	0	1	1	1	0	0	L	L	H
0	1	0	1	0	1	0	L	H	L
0	1	1	1	0	0	0	L	H	H
1	0	0	0	1	1	0	H	L	L
1	0	1	0	1	0	0	H	L	H
1	1	0	0	0	1	0	H	H	L
0	0	0	0	0	0	0	Z	Z	Z
0	0	0	1	1	1	0	L	L	L
1	1	1	0	0	0	0	H	H	H
X	X	X	X	X	X	1	Z	Z	Z

H=V_{cc}, L=RETURN, X=IRERELEVENT, Z=HIGH IMPEDENCE (OFF)

TABLE 4. PIN ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	V _{ssc}	26	GND
2	V _{oc}	25	V _{uc}
3	V _{cc}	24	V _{lc}
4	N/C	23	V _{sd}
5	V _{ssB}	22	GND
6	V _{OB}	21	V _{UB}
7	V _{cc}	20	V _{LB}
8	V _{ssA}	19	GND
9	V _{OA}	18	V _{UA}
10	N/C	17	V _{LA}
11	V _{cc}	16	V _{LPI}
12	V _B	15	NO PIN
13	V _z	14	NO PIN

NOTE: Pins 3, 7 and 11 are internally connected.

ORDERING INFORMATION

PWR-82332-XX0

Reliability Grade:*
0=Standard DDC Procedures
1=B-Level, Military processing available
2=B-level, Military procedures available
but without QCI testing

Temperature Range:
1=-55 to +125°C
3= 0 to +70°C

* For space flight hardware, please refer to NASA Drawing
#SSQ 22691 and consult our factory.

NOTES

The information provided in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.



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